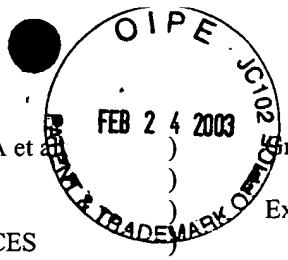
FORM PTO-1083 (modified)

Case Docket No. 15.17/5051



In re the Application of: FURUHATA et al.) Group Art Unit: 2826
Serial No.: 09/599,477)
Filed: June 23, 2000) Examiner: Dickey, T.
For: SEMICONDUCTOR DEVICES)
INCLUDING A NON-VOLATILE)
MEMORY TRANSISTOR)

Box RCE
COMMISSIONER OF PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment and a Request for Continued Examination in the above-identified application.

___ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.

___ A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

___ No additional fee is required.

The fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO PREVIOUSLY PAID FOR		PRESENT EXTRA RATE		ADDIT. FEE	OR	RATE	ADDIT. FEE
TOTAL	35	MINUS	34	=	1	x	$0	OR	x 18	$18
INDEP CLAIMS *	5	MINUS	5	=	0	x	$0	OR	x 84	$
_____ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM						+	$	OR	+ 280	$0
					TOTAL		$0	OR	TOTAL	$18

___ Please charge Deposit Account No. 50-0585 the amount of $___ to cover the extension fee and also the amount of $___ to cover the claim fee. A duplicate copy of this sheet is enclosed.

X A check in the amount of $ 110 to cover the extension fee is enclosed.
X A check in the amount of $ 18 to cover the filing fee for additional claims is enclosed.
X A check in the amount of $ 750 to cover the RCE fee is enclosed.
___ A check in the amount of $ _____ to cover the Information Disclosure Statement fee is enclosed.

X The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. No. 50-0585. A duplicate of this sheet is enclosed.
X Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
X Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

Alan S. Raynes

Dated: February 18, 2003

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Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Box RCE, Commissioner for Patents, Washington, D.C. 20231 on February 18, 2003.

Alan S. Raynes — 2/18/03

Alan S. Raynes — **Date**

#15 Amdt B 3/3/03 aR

15.17/5051

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: FURUHATA et al.	)	Group Art Unit: 2826
Serial No.: 09/599,477	)	
Filed: June 23, 2000	)	Examiner: Dickey, T.
For: SEMICONDUCTOR DEVICES INCLUDING A MULTI-WELL AND SPLIT GATE NON-VOLATILE MEMORY TRANSISTOR STRUCTURE	)	

AMENDMENT

Box RCE
Commissioner for Patents
Washington, D.C. 20231

Dear Sirs:

Applicant filed a Notice of Appeal in response to the Office Action dated June 17, 2002. the Notice of Appeal was mailed to the Office on Monday, Nov. 18, 2002 and was apparently entered by the Office on Nov. 22, 2002. Applicant has filed an Request for Continued Examination and petition for extension of time together with this Amendment. Applicant respectfully requests entry and consideration of the following:

IN THE CLAIMS:

Please add new claim 35 as follows:

--35. (new) A semiconductor device according to claim 33, wherein the non-volatile memory transistor includes a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to act as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer includes at least three insulation layers, wherein a first layer of the at least three insulation layers contacts the floating gate, a third layer of the at least three insulation layers contacts the control gate, and a second layer of the at least three insulation layers is located between the first and third layers, wherein the first, second, and third layers each comprise silicon oxide.--